Device Level Variability in Fin Shapes for 14 Nm FinFET Technologies

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Abstract: FinFET emerges as modification of MOSFET devices to overcome short channel effects and hence becomes hot research issue. The reported work says that Fin shape influences the FinFET performance. In this paper, various fin shapes of FinFET have been analyzed for 14 nm gate length. The different shapes of FinFET are developed by varying the top width of fin. Using 3D simulator visual TCAD, three shapes rectangular, trapezoidal and triangular are designed and simulated. The performance of FinFET is calculated in terms of parameters like V_{TH}, I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio and subthreshold swing (SS) while keeping fin height, gate oxide thickness constant.

Keywords: FinFET, Fin Shape, TCAD, V_{TH} , I_{ON} , I_{OFF} , I_{ON} / I_{OFF} and SS.

Introduction

Gordon Moore predicted in 1965, that number of transistors on integrated circuit would be doubled in every 18 months [1]. The industry is following this trend since then and as a result, numbers of transistors are increasing day by day and channel length of devices has been shrinking constantly for the fabrication of fast and compact devices [2],[3]. This shrinkage had lead to an increase in leakage current, subthreshold swing and short channel effects [4] like drain induced barrier lowering (DIBL), surface scattering, velocity saturation, impact ionization, hot iron effect etc. In 1990s, FinFETs [5]-[7] were classified as the solution of SCEs at University of Berkley, California by Dr. Chenming Hu and his colleagues.

The studies focusing on shape of FinFET had been published in recent years. In [8], the fabrication of FinFET at 70 nm technology was done and concluded that the fin with sharp corners have high gate leakage currents. By reducing width of fin, it gave smooth corners and hence gate leakage current reduced. It also improved subthreshold swing and DIBL. Zhihao et al. in their work [9], designed 10 nm FinFETs and studied effects of shape of fin. NEGF and Nano TCAD were used for calculations to study analog as well as digital performances. Authors in [9], described that FinFET having rectangle shaped Fin performed better than non-rectangular shaped Fin. But for low power applications, trapezoidal shaped fin is preferred. In reported work [10], 25 nm bulk FinFET was discussed and the parameters i.e. ON-state current, SS, DIBL were considered w.r.t. various angles of fin. It had been concluded that for the electrical characteristics, an ideal rectangular fin shape becomes necessary. Greg et al. in their work [11] for 32 nm FinFET studied the effect of line edge roughness up to amplitude of 1 nm and found that the same was negligible for spacer defined FinFETs and non-negligible for resist defined. It had been shown in the results that with smaller magnitude, the variability in line edge roughness was similar on performance of circuit device. The authors [12] implemented SCEs sub models and proposed a unified compact model of FinFET which uses four different parameters to calculate electrical behavior of devices. The authors predicted accurate characteristics of different structures of FinFETs in terms of V-I. It had been shown that the fin shape impact is considerable on the performance of leakage. It had also been illustrated that when base width is kept same in case of rectangular and triangular fins of 22 nm FinFETs, then with doping optimization, the leakage current is reduced by 70% in case of triangular fin. The literature[13] described that it had been shown that the device parameters i.e. oxide thickness, drain doping concentration, effective mobility, junction depth and temperature affects the leakage currents like GIDL and subthreshold more in the case of triangular FinFET. On comparing 22 nm FinFETs, triangular shaped fin is preferred over rectangular as it gives 10% reduction in leakage current. The authors [14], preferred trapezium PC-FinFETs (partial cylindrical) for the applications of multi threshold and low leakage. When 22 nm bulk trapezium PC-FinFET and inverse trapezium PC-FinFET were compared, the authors analyzed that Fin shape impact was considerable on leakage performance. In [15], the investigation of 10 nm U-FinFET structure was described using TCAD tool. U-FinFET resulted in increase of channel length as compared to conventional FinFET. The reduction had been found in the SS value and leakage current. In reported work [16], SOI and bulk FinFETs had been evaluated. When performance had been calculated in terms of threshold voltage and sub-threshold swing, bulk FinFET resulted in improvement in bulk FinFET as compared to SOI FinFET. But SOI FinFET had better sub-threshold value and it is preferred because isolation had been provided by SOI.

In this work, the device level variability in fin shapes has been analyzed. The designing of FinFET with different fin shapes with gate length 14 nm has been described in this work. These fin shapes are rectangular fin, trapezoidal fin and triangular fin and it has been shown in Fig. 1 respectively.

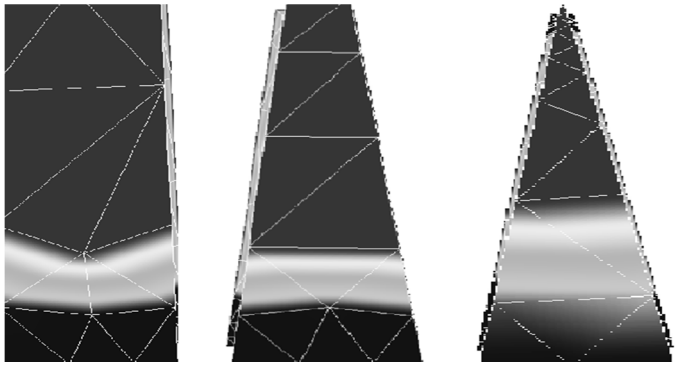


Fig. 1. Rectangular fin, Trapezoidal fin and Triangular fin resp.

The paper further includes the section II describes the Fin shape device methodology. In the section III, simulations are realized and in the section IV, their results and discussions are presented. Then the impact of Fin Shape has been explained in the conclusion and the future scope is discussed.

Device Methdology

For the designing and simulation purpose, GDS2Mesh 3D Modeller Technology Computer Aided Design Simulator Manager (TCAD) has been used. The bottom fin width (Wbottom) has taken same in all three cases i.e. 15 nm. The shape of FinFET can be developed by varying the top fin width (Wtop). To make rectangular fin, the top fin width has been taken same as the bottom fin width i.e. 15 nm. In case of trapezoidal fin, the top width has set as 5 nm and to make triangular fin, the top fin should be zero. In this work,the top width of triangular fin had taken as 0.001 nm (~ 0 nm). This can be summarized in Fig. 2.

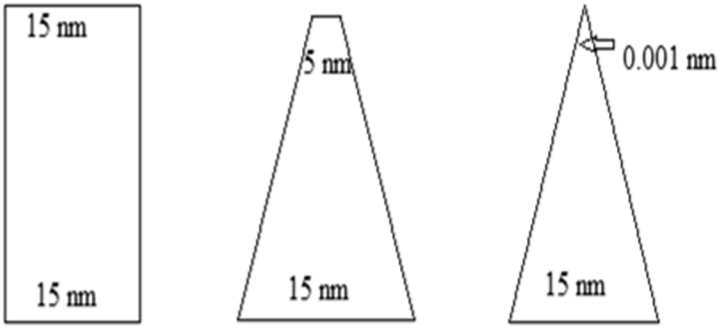


Fig. 2. Fin Shapes with their respective top and bottom width.

The simulations have been realized by keeping some parameters of device constant in all cases. The device parameters includes the information like design architecture parameters i.e. length, width and height in fin etc. Table 1, given below lists the various parameters used for simulation.

Table 1. Device Parameters taken for simulation

Parameters	Description	Values
H_{fin}	Height of fin	30 nm
W_{bottom}	Bottom Width of fin	15 nm
Lmd	Lambda	7 nm
T_{OX}	Thickness of gate oxide	1 nm

Simulations

To make 3D structure, layout diagram is required. Basically, it depicts the way in which the parts of device are arranged or laid out. It also represents the layer information of device. The layout diagram used for all shapes of 14 nm FinFET is shown in Fig. 3.

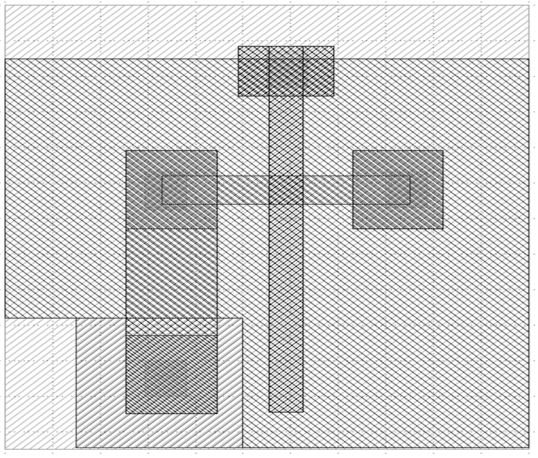


Fig. 3. Layout diagram for 14 nm FinFET

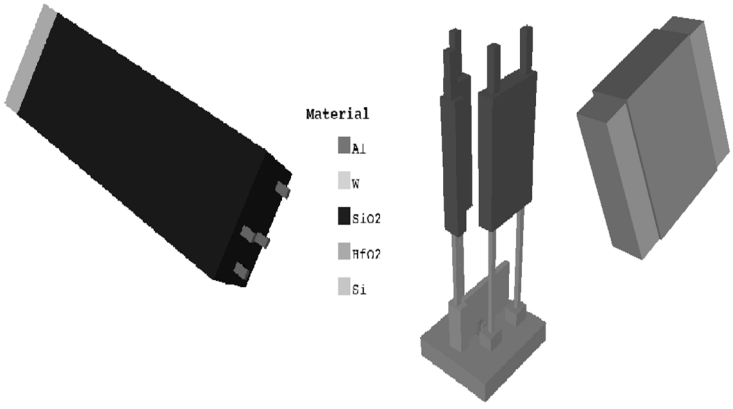
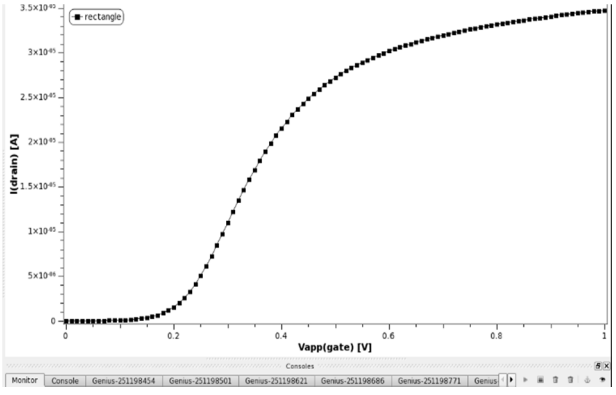


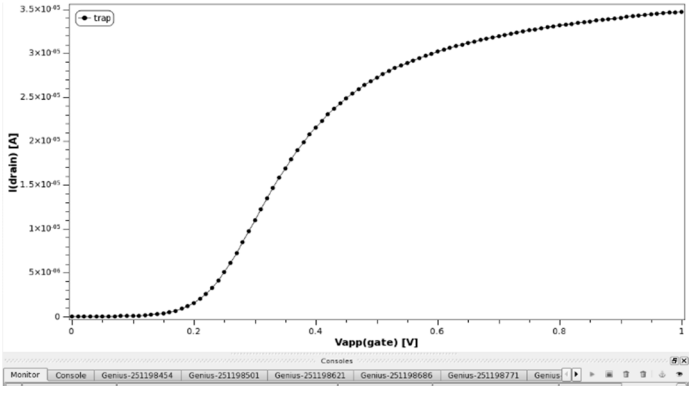
Fig. 4 (a) Whole FinFET (b) Metallic contact and (c) Active fin.

The different models can be used for the simulation purpose. The designed FinFET structure is shown in Fig. 4 (a). By removing the outer layers, the metallic contact and active fin is visible as shown in Fig. 4 (b) and Fig. 4 (c). In Fig. 4 (c), the active fin shown is for rectangular shape. This procedure is same for all the shapes.

Results and Discussion

All designed FinFETs' performance has been analyzed through 3D TCAD as described in above section. The performance of the designed FinFETs with different Fin Shapes i.e. rectangular, trapezoidal and triangular for 14 nm has been analyzed in form of threshold voltage (V_{TH}), ON-current (I_{ON}), OFF-current (I_{OFF}), ratio of ON-OFF-current (I_{ON}/I_{OFF}) and subthreshold swing (SS) by keeping the all other parameters like fin height, gate oxide thickness constant in all cases. The minimum V_{gs} voltage which is used to establish a conducting way between drain as well as source terminals is called threshold voltage. The ON and OFF states correspond to high and low voltages states of internal circuit nodes. The drive current is defined as the drain current of a transistor with gate and drain connected to the supply voltage and source grounded, it is also referred to as on-state current. The channel leakage current is defined as the drain current with drain connected to the supply voltage and gate & source grounded. For higher performance, the figure of merit is I_{ON}/I_{OFF} ratio and it is more when on-current is more and off-current is less. More I_{ON}/I_{OFF} ratio means better performance. The graph of I_{ds} vs V_{ds} when plotted with logarithmic (base 10) axis for I_{ds} subthreshold swing, it is found as the straight line approximate the subthreshold current. Subthreshold swing is inverse of subthreshold swing and expressed in units of mV/decade. The transfer characteristics of all the FinFETs have been shown by plotting the graph between the drain current and voltage gate in the Fig. 5.





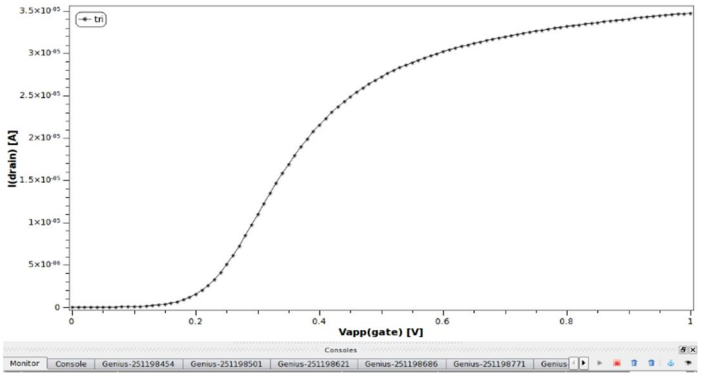


Fig. 5. Transfer Characteristics of rectangular, trapezoidal and triangular FinFETs

ON-current (I_{ON}) is dependent on the fin height which is kept same in all the shapes and fin width which is varying in this work. The calculated parameters of all FinFETs after the simulation are given in the Table 2. It shows that I_{ON} and I_{OFF} is minimum in case of triangular FinFET and I_{ON}/I_{OFF} ratio is also maximum. Thus, Triangular FinFET is preferred over other shapes because of highest figure of merit i.e. I_{ON}/I_{OFF} ratio. I_{OFF} is used to measure leakage in off-state of device. It is dependent on the top fin width and it reduces with the reduction in W_{top}. Hence, OFF-current (I_{OFF}) is minimum in case of triangular shape.

TABLE II. Results obtained of all simulated FinFETs

Parameters/Shapes	Rectangular	Trapezoidal	Triangular
V_{TH}(V)	0.24	0.24	0.24
I_{ON}(A)	3.475e-05	2.626e-05	8.778e-06
I_{OFF}(A)	2.608e-09	7.275e-10	1.307e-10
I_{ON}/I_{OFF}	1.332e+04	3.609e+04	6.716e+04
Subthreshold Swing(mV/dec)	70	68	66

The output characteristics of rectangular FINFET are plotted by the graph between drain current and drain voltage at different values of gate voltage (V_g) which is shown in Fig. 6. Similarly the output characteristics of trapezoidal FINFET and triangular FINFET are plotted by the graph between drain current and drain voltage at different values of gate voltage (V_g). This has been shown in Fig. 7 and Fig. 8 respectively.

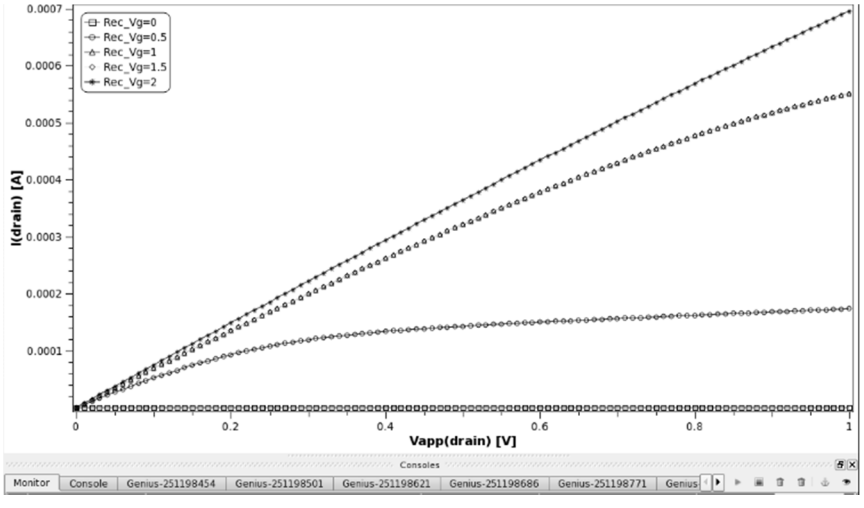


Fig. 6. Transfer Characteristics of rectangular FinFETat different values of V_g

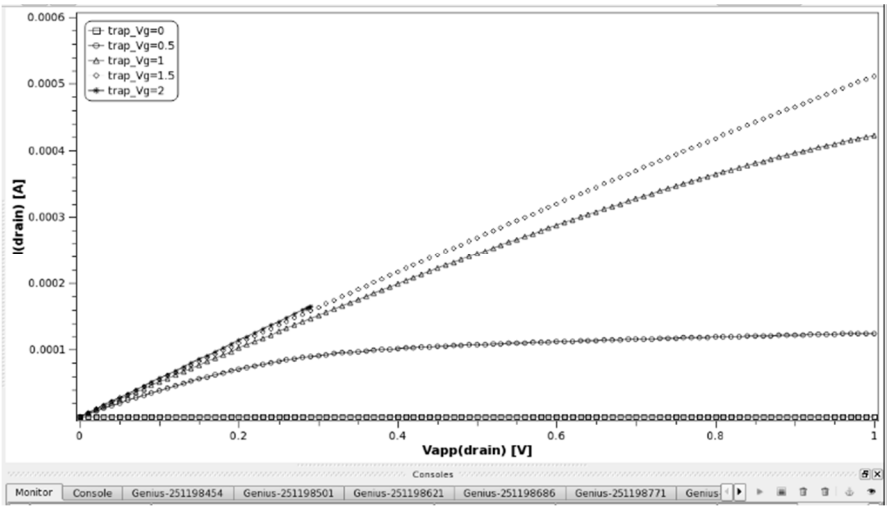


Fig. 7. Transfer Characteristics of trapezoidal FinFETat different values of V_g

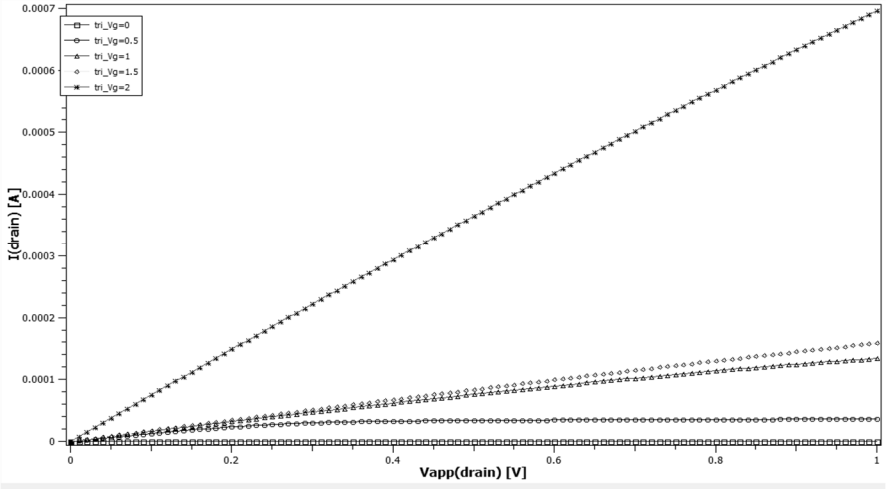


Fig. 8. Transfer Characteristics of triangular FinFET at different values of V_g

Conclusion

It can be concluded that the Fin shape has a considerable impact on the device performance. Fin width varies according to shape. In this work, three different Fin Shapes i.e. rectangular, trapezoidal and triangular were designed and analyzed with the gate length 14 nm. The performance was analyzed in terms of threshold voltage (V_{TH}), ON-current (I_{ON}), OFF-current (I_{OFF}), ratio of ON-OFF-current (I_{ON}/I_{OFF}) and subthreshold swing (SS). The triangular fin shape FinFET showed an improvement in performance as compared to other two shapes studied. This is due to reduction in leakage current, thus it possess maximum I_{ON}/I_{OFF} ratio. As technology is scaling day by day, the triangular fin shape can be a preferable option.

The variation of angles of fin can be studied in future as smoothening the angle gives better results. For high performance, multi fin FinFET can be designed by the combining of different fin shapes. To improve the SCEs and drive current, the triangular fin shape can be used with the mixing of another shape.

References

[1] J.P. Colinge, “FinFETs and other Multi-Gate Transistors,” Springer, 2008.

[2] C. R. Manoj, M. Nagpal, D. Varghese and V. R. Rao, “Device Design and Optimization Considerations for Bulk FinFETs,” IEEE Transactions on Electronic Devices, vol. 55, no. 2, 2008, pp. 609-615.

[3] J. T. Park and J. P. Colinge, “Multiple-Gate SOI MOSFETs Device Design Guidelines,” IEEE Transactions on Electronic Devices, vol. 49, no. 12, 2002, pp. 2222-2229.

[4] F. D. Agostino and D. Quercia, “Short Channel Effects in MOSFETs,” 2000 [Online]. Available: http://www0.cs.ucl.ac.uk/staff/ucacdxq/projects/vlsi/report.pdf

[5] A. Kumar, B. Kaur and N. Arora, "Evolution of Transistors Technology from BJT to FinFET- A study," International Journal of Computer Applications , International Conference on Advances in Emerging Technology, 2016.
[6] D. Bhattacharya and N. K. Jha, "FinFETs: From Devices to Architectures", Hindawi Publishing Corporation, Advances in Electronic, vol. 2014, Article ID 365689 [Online]. Available: http://dx.doi.org/10.1155/2014/365689
[7] N. Horiguchi et al. , "FinFETs and Their Futures, Research Gate", 2011 [Online]. Available: https://www.researchgate.net/publication/226551754
[8] W. Xiong et al. , "Improvement of FinFET Electrical Characteristics by Hydrogen Annealing," IEEE Electron Device Letters, vol. 25, no.8, 2004, pp. 541-543.
[9] Z. Yu, S. Chang, H. Wang, J. He and Q. Huang, "Effects of Fin Shape on sub-10nm FinFETs," Springer, 2015.
[10] Y. Li and C. H. Hwang, "Effect of Fin Angle on Electrical Characteristics of Nano-Scale Round-Top-Gate Bulk FinFETs," IEEE Transactions on Electrons Devices, vol. 54, no. 12, 2007, pp. 3426-3429.
[11] G. Leung, L. Lai, P. Gupta and C. O. Chui, "Device- and Circuit- Level Variability Caused by Line Edge Roughness for Sub-32-nm FinFET Technologies," IEEE Transactions on Electron Devices, vol. 59, no. 8, 2012, pp. 2057-2063.
[12] B. D. Gaynor and S. Hassoun, "Fin Shape Impact on FinFET leakage with Application to Multithreshold and Ultra low-Leakage FinFET Design," IEEE Transactions on Electron Device, vol. 61, no. 8, 2014, pp. 2738-2744.
[13] D. Abraham, A. George and D. Gopinadh, "Effects of Fin Shape on GIDL and Subthreshold Leakage Currents," International Journal of Science Technology & Engineering, vol. 1, no. 10, 2015.
[14] A. Jyothi, T. E. A. Khan, N. Kuruvilla and T. A. S. Hameed, "Impact of Fin Shape on FinFET Performance," International Journal of Computer Applications, International Conference in Emerging trends in Technology and Applied Science, 2015.
[15] W. C. Zhou, P. F. Wang and D. W. Zhang, " A Sub-10 nm U shape FinFET Design with suppressed leakage current and DIBL effect," IEEE Conference Publications, China Semiconductor Technology International Conference , 2015, pp. 1-3.
[16] R. Deshmukh, A. Khanzode, S. Kakde and N. Shah, " Compairing FinFETs: SOI vs Bulk; Process Variability, Process Cost, And Device Performance," IEEE International Conference on Computer, Communication and Control, 2015, pp. 1-4.